**SARASWATI MAHILA MAHAVIDHYALAYA, PALWAL**

**LESSON-PLAN**

**Class: BCA IST YEAR Semester: ODD**

**Subject: LOGICAL ORGANISATION OF COMPUTER-I**  **Session: 2020-21**

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| **Lecture Number** | **TOPIC** |
|  | **UNIT 1** |
| **L 1-20** | **Number system and its types.** |
| **Decimal number system and its conversion .** |
| **Octal number system and its conversion.** |
| **Binary number system and its conversion.** |
| **Hexadecimal number system and its conversion.** |
| **Conversion between number systems.** |
| **Binary operations.** |
| **Addition in binary.** |
| **Continue.** |
| **Subtraction in binary.** |
| **Complement forms.** |
| **Multiplication an divison in binary .** |
| **Fixed representation of numbers.** |
| **Floating point representation of numbers.** |
| **Bcd codes.** |
|  | **Continue..** |
| **Error detecting codes.** |
| **Error correcting codes.** |
| **Character representation codes.** |
| **ASCII-7** |
| **ASCII-8** |
| **EBCDIC** |
| **Unicode.** |
| **REVISION AND TEST.** |
|  | **UNIT 2** |
| **L 21-35** | **Boolean Algebra** |
| **Continue.** |
| **Theorems of Boolean algebra.** |
| **Continue.** |
| **Boolean Functions.** |
| **Truth table of Boolean functions.** |
| **Canonical forms of Boolean functions .** |
| **Continue.** |
| **Standard forms .** |
| **Simplification of Boolean functions.** |
| **Continue.** |
|  | **Continue.** |
| **Venn-Diagram.** |
| **k-map.** |
| **Continue..** |
| **k-map using sop form.** |
| **k-map using pos form.** |
| **Continue.** |
| **CLASS TEST** |
|  | **UNIT 3** |
| **L 36-55** | **Introduction to gates.** |
| **Basic gates(AND ,OR,NOT)** |
| **Universal gates .** |
| **Nand and its implementation .** |
| **Nor and its implemention .** |
| **Xor and its working.** |
| **Xnor and its working .** |
| **And-or-invert and its implementation.** |
| **Or-and-invert and its implementation.** |
| **Implementation of digital circuit.** |
| **Multilevel NAND Circuit.** |
| **Multilevel NOR circuit.** |
|  | **CLASS TEST** |
|  | **UNIT 4** |
| **L 56-70** | **Combinational logic its characteristic .** |
| **Its design and analysis procedure.** |
| **Revision and Test.** |
| **Half adder and its implementation.** |
| **full adder and its implementation.** |
| **Half subtractor and its implementation.** |
| **full adder and its implementation.** |
| **Parallel binary adder /subtractor.** |
| **Encoders.** |
| **Decoders.** |
| **Multiplexer.** |
| **Demultiplexer.** |
| **Code convertor.** |
| **Comparator.** |
| **Bcd to 7 segment decoder.** |
| **CLASS TEST** |
| **REVISION** |

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